

**REMARKS**

Applicants have amended their title to address the Examiner's objection. Independent claims 1 and 6 have been amended to recite that the interconnection is "formed horizontally with respect to the semiconductor substrate" and that "a width of the extended portion is below a width of the main interconnection portion."

**Rejection Under 35 U.S.C. §103**

Claims 1-8 are rejected under 35 U.S.C. §103(a) as being unpatentable over Bease et al. (U.S. Patent No. 6,239,025) taken with Tsukamoto (U.S. Patent No. 6,040,224) and Wu (U.S. Patent No. 6,017,815).

**A. The Invention**

In the semiconductor of the present invention, the interconnection has an extended portion provided at an end part of the main interconnection portion and extended perpendicularly in the extending direction of the main interconnection portion. Also, the width of the extended portion in the extending direction of the main interconnection portion is below the width of the main interconnection portion. As recited in claims 1 and 6, the interconnection is formed horizontally with respect to the semiconductor substrate.

According to this feature of the present invention, the interconnection groove for burying the interconnection can be formed, and yet the shrinkage of the pattern end due to the proximity effect upon the exposure is effectively suppressed. Thus, the reliability of the electrical contact with the upper interconnection connected to the end part of the interconnection can be higher. The width of the extended portion is set below the width of the main interconnection portion, so

that the interconnections can be arranged in a small pitch without decreasing the breakdown voltage between the adjacent interconnections (*see, e.g.*, page 9, lines 7-15 of the specification).

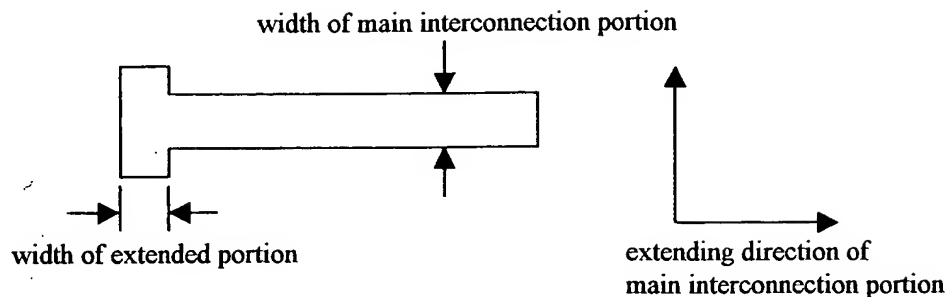
B. The Prior Art and Applicants' Response

Bease discloses in, *e.g.*, FIG. 4H, the semiconductor device including contacts 46 buried in insulating film 12. Contacts 46 include a lower cylindrical portion and an upper portion comprising an enlarged head (column 3, lines 34-36). However, in Bease, contacts 46 are formed *vertically* with respect to the semiconductor substrate 4 (*see, e.g.*, FIG. 4H).

The object of the present invention is to prevent the shrinkage of the pattern end due to the proximity effect upon the exposure for forming the interconnection groove in order to prevent the defective contact electrically connected to the end part of the interconnection. Thus, in the present invention, the interconnection is formed *horizontally* with respect to the semiconductor substrate as recited in claims 1 and 6. Bease clearly differs from the present invention and does not provide any motivation for the present invention.

Tsukamoto discloses, *e.g.*, in FIGs. 3 and 4, the semiconductor device including the gate electrode having a narrow line portion 1 of a first width  $a_1$ , and a wide line portion 3 integrally formed on at least one end of the narrow line portion 1 and having a second width  $b$  larger than the first width  $a_1$ . The second width  $b$  is a width of the wide line portion 3 in the direction perpendicular to the extending direction of the narrow line portion 1 (*see, e.g.*, FIGs. 3 and 4).

However, as described above, the present invention has a feature that the width of the extended portion in the extending direction of the main interconnection portion is below the width of the main interconnection portion, as shown below:



The Examiner states that the selection of the appropriate width of the extending portion including the width to be below a width of the main interconnect portion would have obvious to one skilled in the art because of Tsukamoto, column 3, lines 50-53. However, Tsukamoto only teaches the relationship between the width  $a_1$  of narrow line portion 1 and the width  $b$  of wide line portion 2 in this disclosure. *Tsukamoto neither teaches nor suggests the relationship between the width  $a_1$  of the narrow line portion 1 and the width of the wide line portion 3 in the extending direction of the narrow line portion 1.*

Additionally, the object of the present invention is to prevent the defective contact electrically connected to the end part of the interconnection. Thus, the semiconductor device according to the present invention includes a second insulating film having a contact hole down to the end part of the main interconnection portion of the interconnection where the extended portion is provided. Tsukamoto neither teaches nor suggests the contact hole formed down to the gate electrode.

Thus, Tsukamoto clearly differs from the present invention and does not provide any motivation for the present invention.

Wu discloses, *e.g.*, in FIGs. 1 and 2 and column 1, lines 19-39, the semiconductor device including the conductive layer 12 having the wide line portion provided at the end thereof, and the insulating film 16 having the via 18 down to the wide line portion of the conductive layer 12.

However, it is apparent from FIG. 2 of Wu that the width of the wide line portion of the conductive layer 12 in the extending direction of the conductive layer 12 is larger than the width of the main portion of the conductive layer 12. In Wu, a border 17 is formed around the via 18 in order to avoid misalignment which may be caused during the stepper or fabrication process (*see, e.g.*, column 1, lines 29-32). Thus, the width of the wide line portion would become larger than the width of the main portion of the conductive layer 12. Wu neither teaches nor suggests the relationship between the width of the main portion of the conductive layer 12 and the width of the wide line portion of the conductive layer 12 in the extending direction of the main portion of the conductive layer 12.

Wu clearly differs from the present invention and does not provide any motivation for the present invention.

### C. Conclusion

In view of the aforementioned amendments and accompanying remarks, Applicants submit that the claims, as herein amended, are in condition for allowance. Applicants request such action at an early date.

If the Examiner believes that this application is not now in condition for allowance, the Examiner is requested to contact Applicants' undersigned attorney to arrange for an interview to expedite the disposition of this case.

Response under 37 C.F.R. §1.111

Attorney Docket No. 032180

Serial No. 10/743,438

If this paper is not timely filed, Applicants respectfully petition for an appropriate extension of time. The fees for such an extension or any other fees that may be due with respect to this paper may be charged to Deposit Account No. 50-2866.

Respectfully submitted,

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